



iMAPS 2016 HiTEC

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Electrical Performance of a High Temperature 32-I/O HTCC Alumina Package

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Outline

- Background
 - 500°C SiC electronics and sensors
 - 96% alumina and thick-film metallization based packaging system for 500°C applications
 - Challenges of thick-film/alumina systems
 - Dielectric properties of selected HTCC (high temperature co-fired ceramics) alumina
- Design of a prototype HTCC alumina 32-I/O package
- Electrical performance of HTCC 32-I/O package
 - DC insulation resistance of neighboring I/Os
 - AC parasitic of neighboring I/Os
- Test with SiC JFET ICs
- Summary and Discussions

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Background

500°C SiC electronics and sensors in development

- JFETs based circuits demonstrated at NASA GRC
- MEMS based pressure sensors and Schottky diode based gas chemical sensors developed at NASA GRC
- NASA applications include aerospace engine monitoring/control, long term Venus probes
- Packaging system needed

Previous 96% alumina and thick-film metallization based prototype packaging system

- Tested with SiC electronics at 500°C for over 10,000 hours
- Lab steps involved in package integration, thermo-dynamic stability of binder components in thick-film materials

Co-fired Pt/alumina material system

- Selected HTCC alumina dielectrically outperforms 96% alumina
- Pt was proposed as co-fired conductor

Dielectric properties of HTCC alumina material

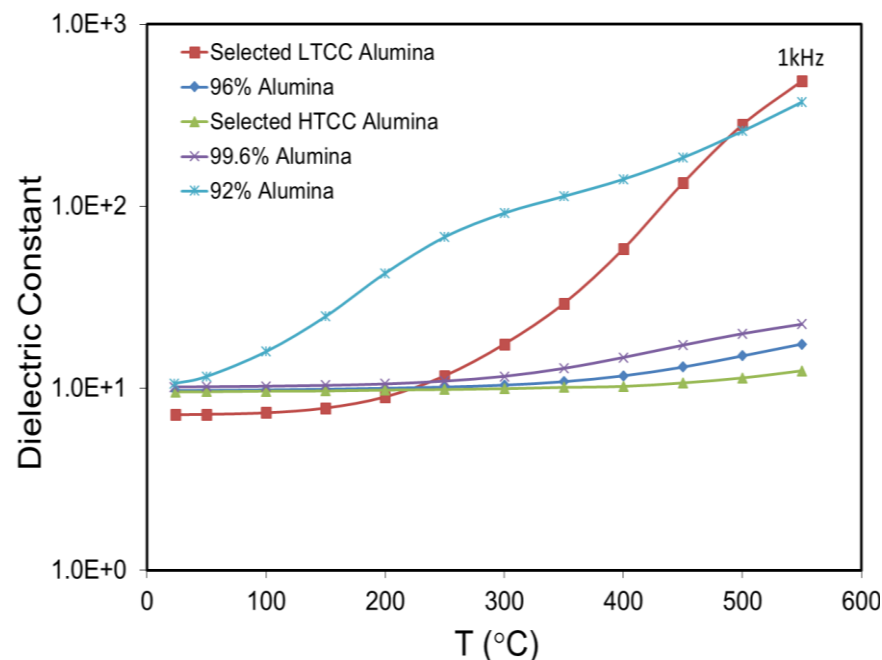
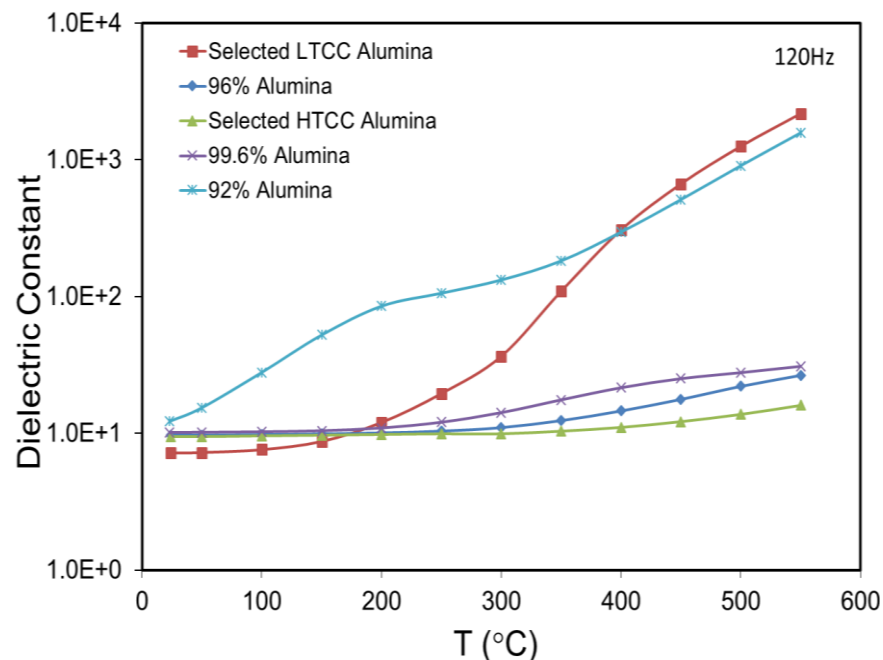
Dielectric properties of packaging Substrate at elevated temperatures is critical to parasitic packaging effects

- Low dielectric constant – low parasitic capacitance
- Low AC conductivity / low dissipation factor / high quality factor – high parasitic resistance
- Stability with temperature increase

High temperature co-fired (HTCC) alumina

- Co-fired at $T > 1500^{\circ}\text{C}$
- A few percent of glass used in co-fired alumina systems
- Dielectric performance of selected HTCC alumina tested at high temperatures
- Pt metallization
 - Chemically stable at high temperatures
 - Low CTE ($8.8 \times 10^{-6}/^{\circ}\text{C}$)
 - Aluminum oxide for binder - Thermal dynamically stable
 - Alloy with Au, Au is always surface rich at elevated temperatures

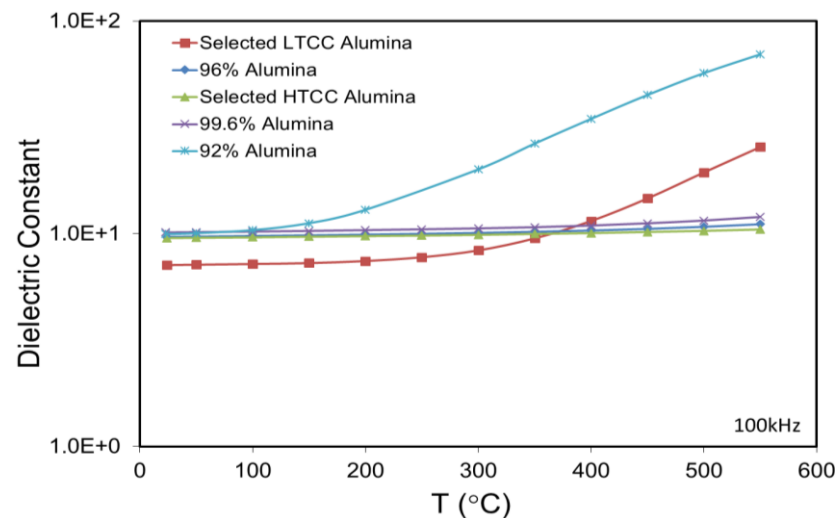
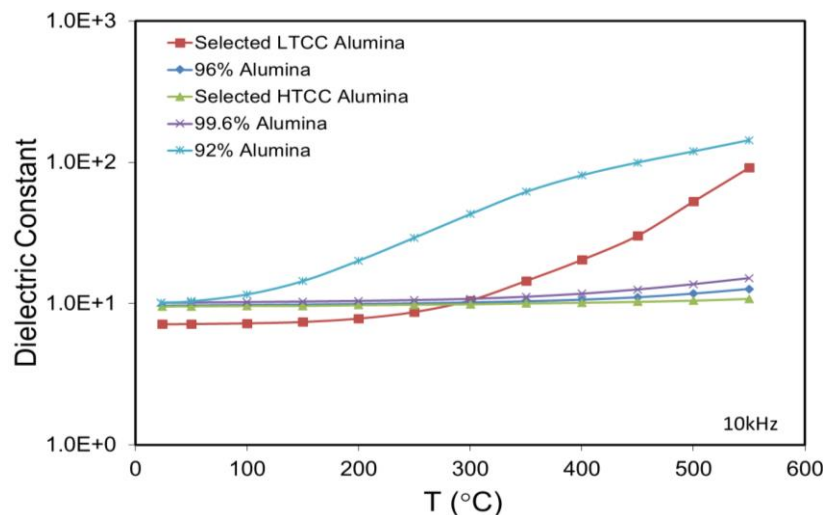
Dielectric constant of HTCC alumina material



Compared with 96% alumina:

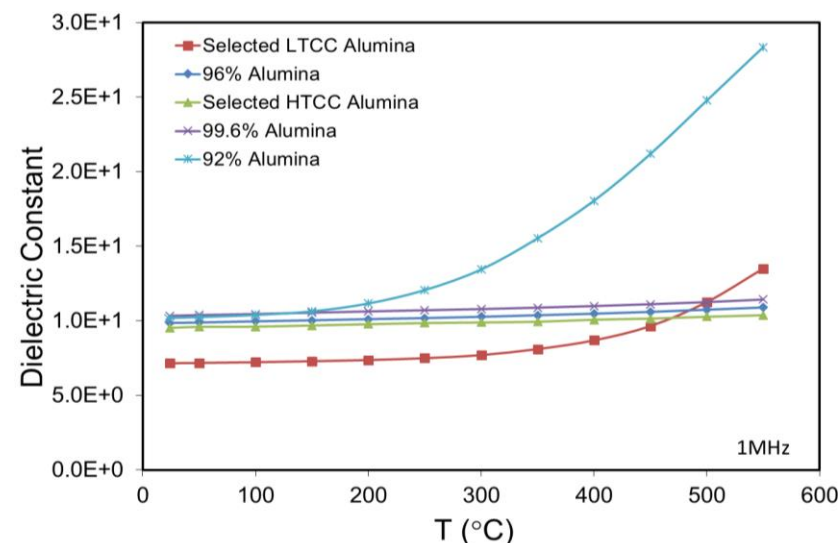
- Dielectric constants of 92% and 99.6% alumina are higher and increases more at 120Hz and 1kHz
- Dielectric constant of HTCC alumina is lower and increases less at 120Hz and 1kHz

Dielectric constant of HTCC alumina material

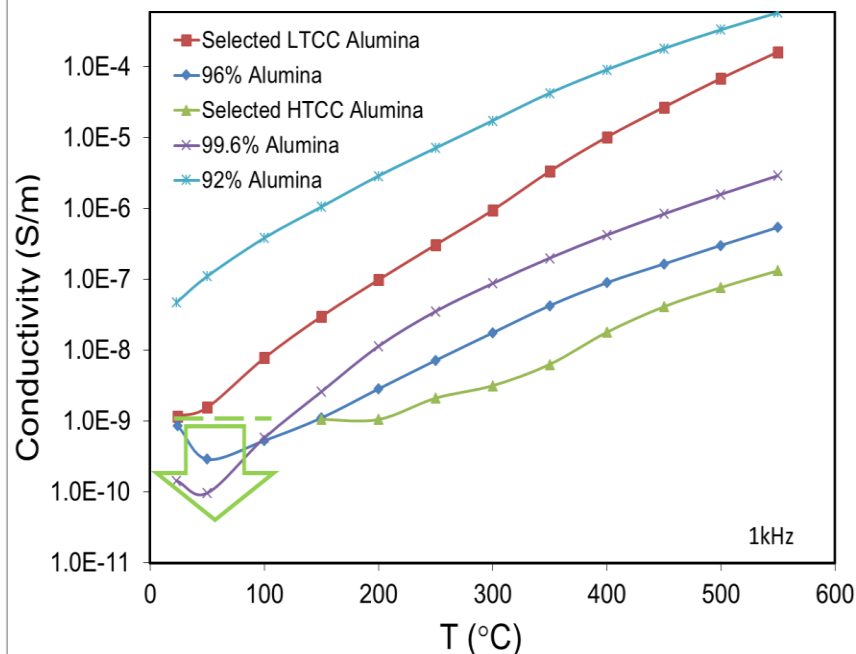
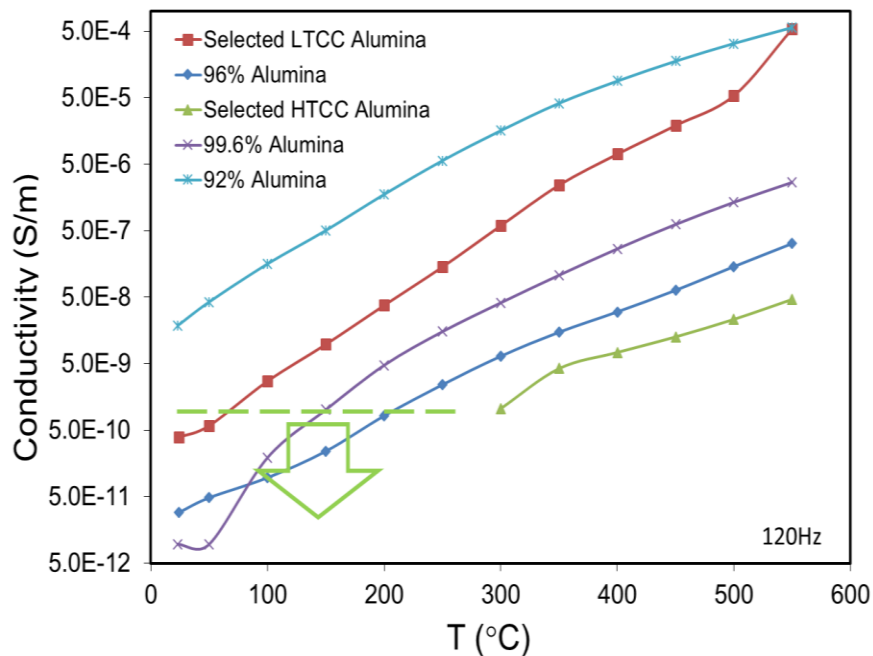


Compared with 96% alumina:

- Dielectric constants of 92% and 99.6% alumina are higher and increase more at 10kHz, 100kHz, and 1 MHz
- Dielectric constant of HTCC alumina is lower and increases less at 10kHz, 100kHz, and 1MHz



AC conductivity of HTCC alumina material

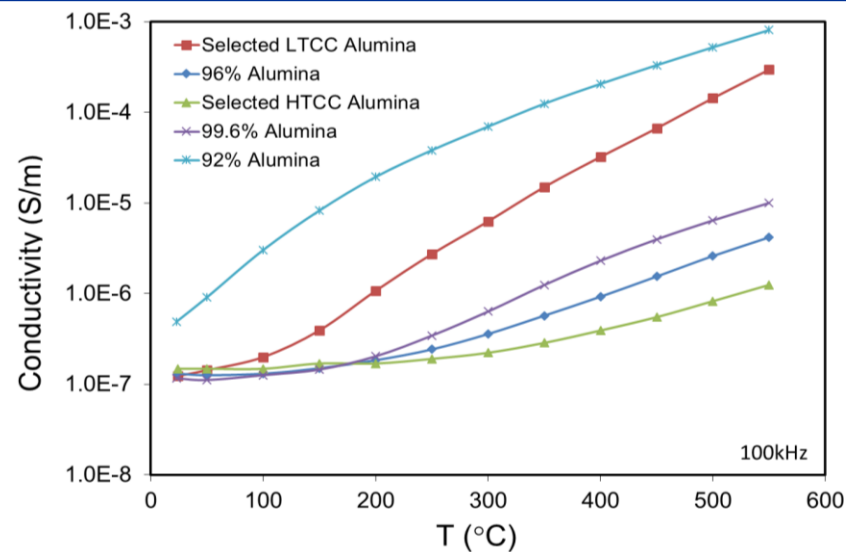
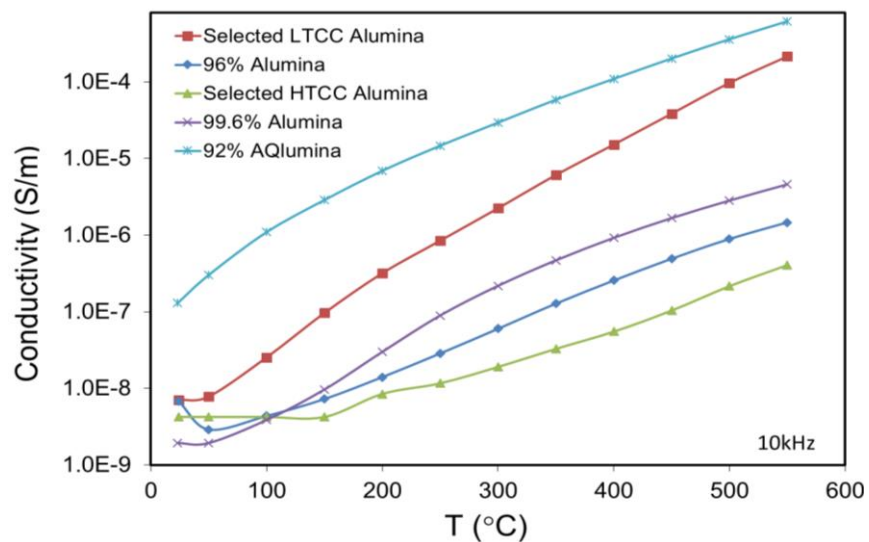


Compared with 96% alumina:

- Conductivities of 92% and 99.6% alumina are higher at temperatures above 100°C at the frequencies of 120Hz and 1kHz
- Conductivity of HTCC alumina is ~ an order of magnitude lower at temperatures above 300°C at the frequencies of 120Hz and 1kHz

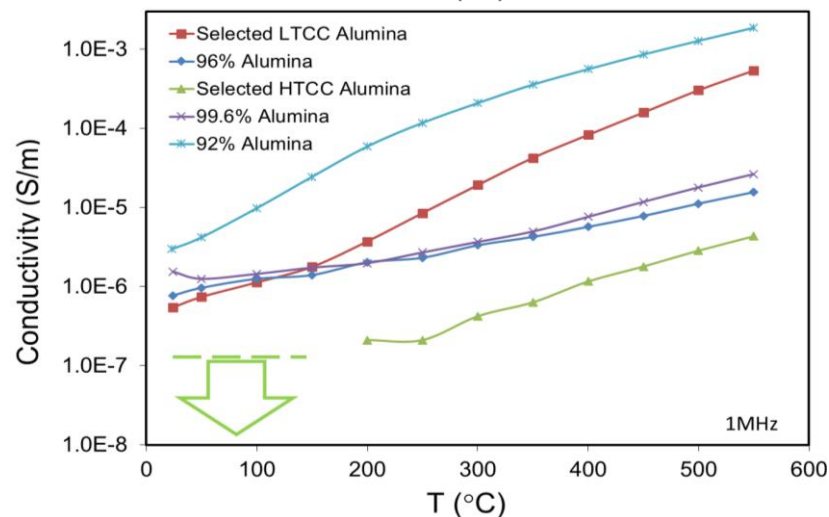
Chen, 2012 HiTEC, 2007 ICEPT

AC conductivity of HTCC alumina material



Compared with 96% alumina:

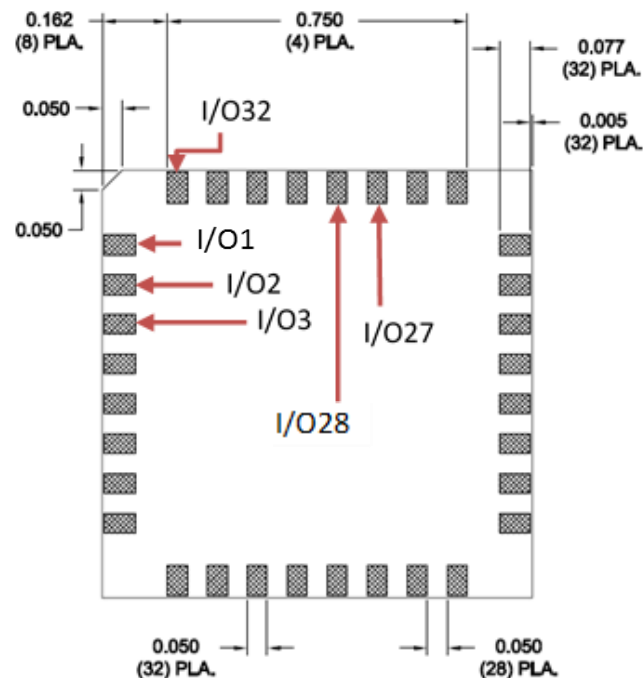
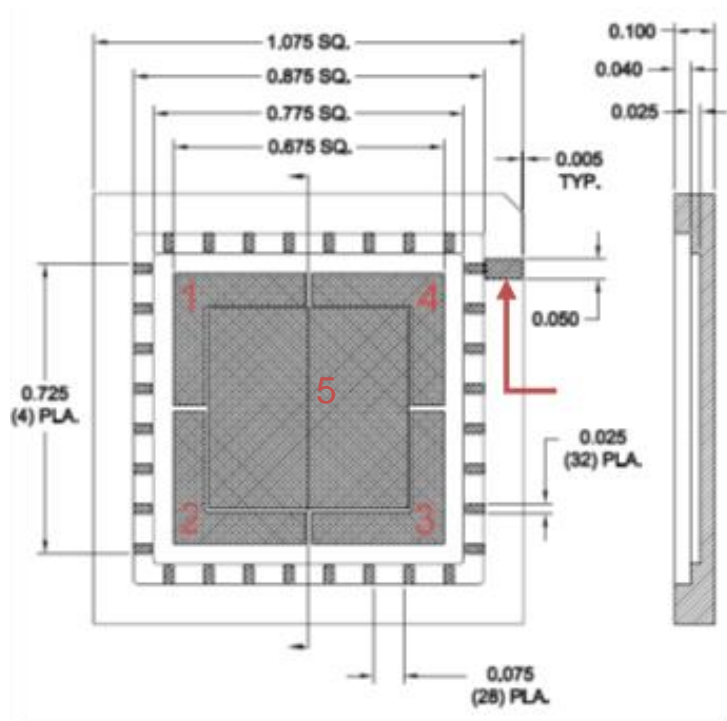
- Conductivities of 92% and 99.6% alumina are higher at temperatures above 200°C at the frequencies of 10kHz, 100kHz, 1MHz
- AC conductivity of HTCC alumina is always lower and increases less with T at 10kHz, 100kHz, and 1 MHz at T > 200°C



Chen, 2012 HiTEC, 2007 ICEPT

OAI HTCC Alumina 32-I/O Package - Design

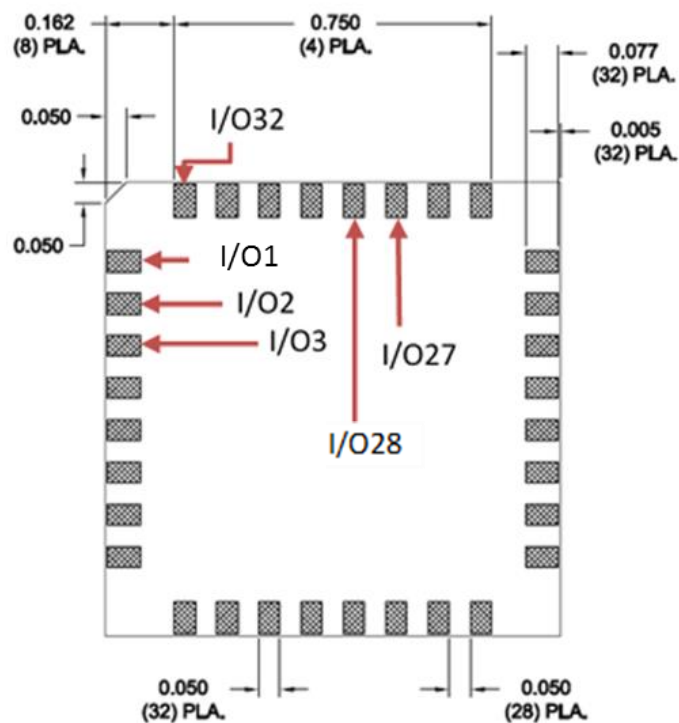
Design of HTCC Pt / Alumina Package



- 92% HTCC alumina co-fired with Pt conductor
- Pt via for vertical electrical connection
- Surface mount, 32 I/Os for low power low frequency 500°C SiC ICs
- Capable of multichip mixture with five separate substrate bias

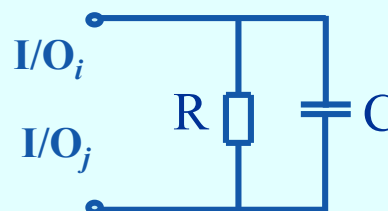
HTCC Alumina Package – Equivalent Circuit

Parasitic R//C of Neighboring I/Os



1.07 inches

Parasitic Equivalent



R//C model

R – DC leakage and AC dielectric loss

C – Dielectric polarization

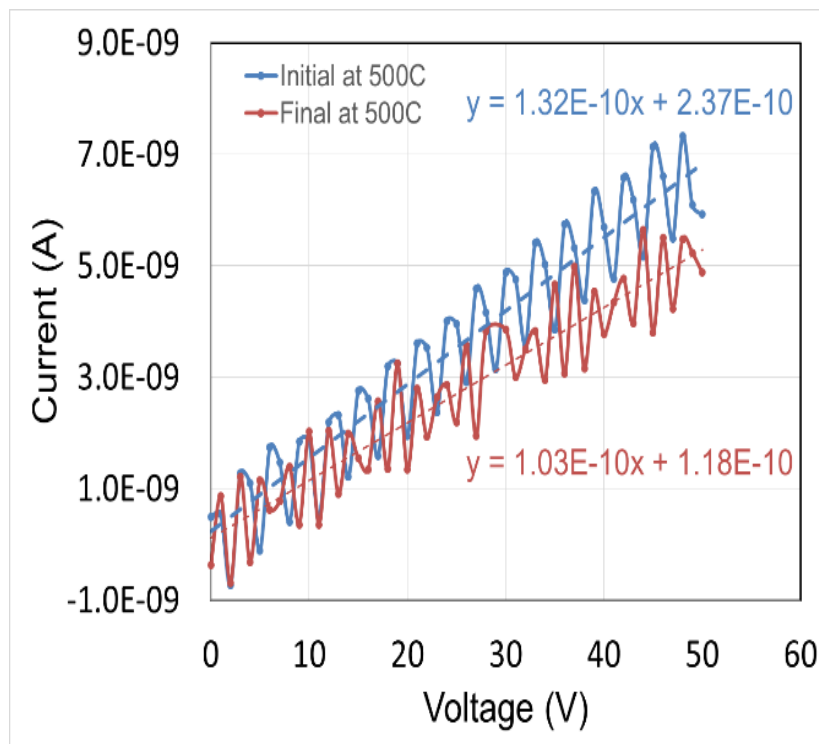
$$1/Z(T, \omega) = G(T, \omega) + j\omega C(T, \omega)$$

R//C measured between I/O1 - I/O2, and I/O2 - I/O3

- I/O1 connected to all five bias pads
- DC resistance measured separately

HTCC Alumina Package – DC Resistance

DC Resistance of Neighboring I/Os



DC I - V Curves

- I-V curve between I/O27 and I/O28
- 500°C
- Wide DC bias range: 0 - 50V
- SMU: integration time 16.67 msec, time delay 0.1 sec
- I/O28 not connected to SiC die, I/O27 connected to isolated two-terminal test structure on SiC die
- Package mounted on PCB
- Slope of linear fits: 7.6 GΩ initially 9.7 GΩ after 69.4 hrs
- DC resistance slightly underestimate
- Noise from running oven

HTCC Alumina Package – AC Parasitic R//C

AC Parasitic Capacitance and Conductance of Neighboring I/O1 – I/O2

f (Hz) \ T (°C)	T_R	100	150	200	250	300	350	400	450	500	550
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.001	<0.001
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4
	<0.001	0.0013	<0.001	<0.001	<0.001	<0.001	<0.001	0.003	<0.003	<0.003	<0.003
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5
	<0.010	<0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026

> 50°C margin
above 500°C

pF
μS

$C < 1.5$ pF, $R > 20$ MΩ

Usable for many envisioned 500°C SiC ICs

HTCC Alumina Package – AC Parasitic R//C

AC Parasitic Capacitance and Conductance of Neighboring I/O2 – I/O3

f (Hz) \ T (°C)	T_R	100	150	200	250	300	350	400	450	500	550
120	0.7	0.6	0.5	0.4	0.3	0.4	0.4	0.6	0.5	0.6	0.6
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
1K	0.3	0.3	0.4	0.4	0.2	0.4	0.3	0.5	0.3	0.5	0.5
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.0013	0.001	<0.001
10K	0.4	0.3	0.4	0.4	0.3	0.3	0.4	0.4	0.4	0.4	0.3
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
100K	0.3	0.3	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	0.005	0.005	<0.005	<0.005	<0.005	0.005	0.013	<0.010	0.014	0.012	<0.010
1M	0.3	0.4	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	<0.010	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020

> 50°C margin
above 500°C

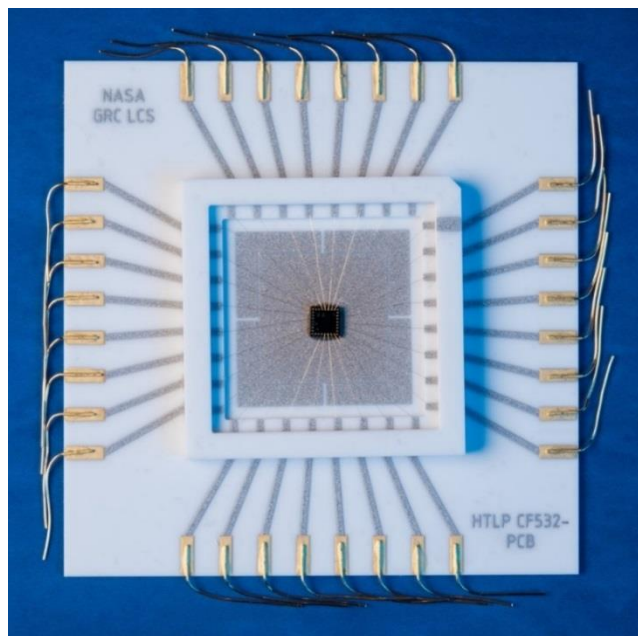
pF
μS

$C < 1.5 \text{ pF}$, $R > 20 \text{ M}\Omega$

Usable for packaging many envisioned 500°C SiC ICs

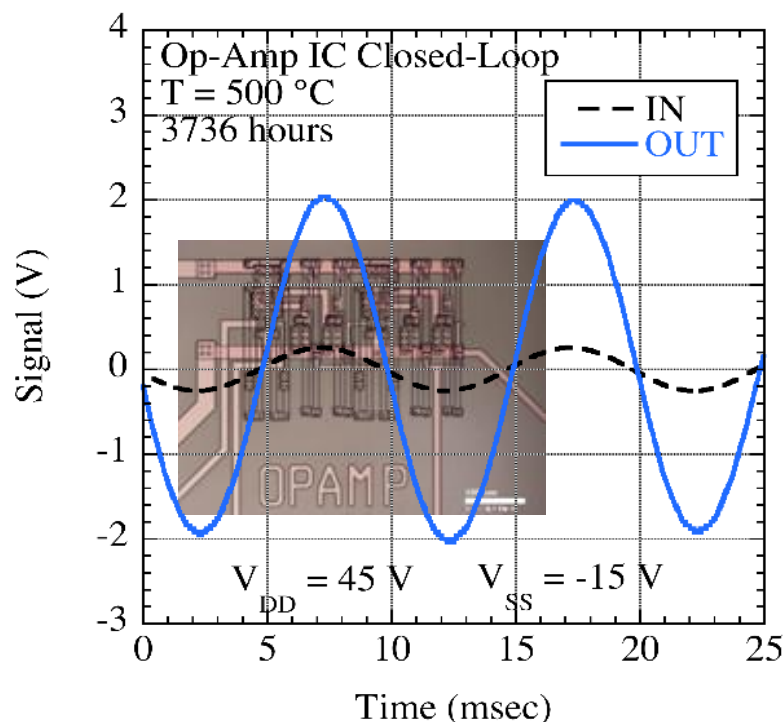
Test with SiC ICs at High Temperature

Test Assembly of a SiC IC with HTCC Alumina Packaging System

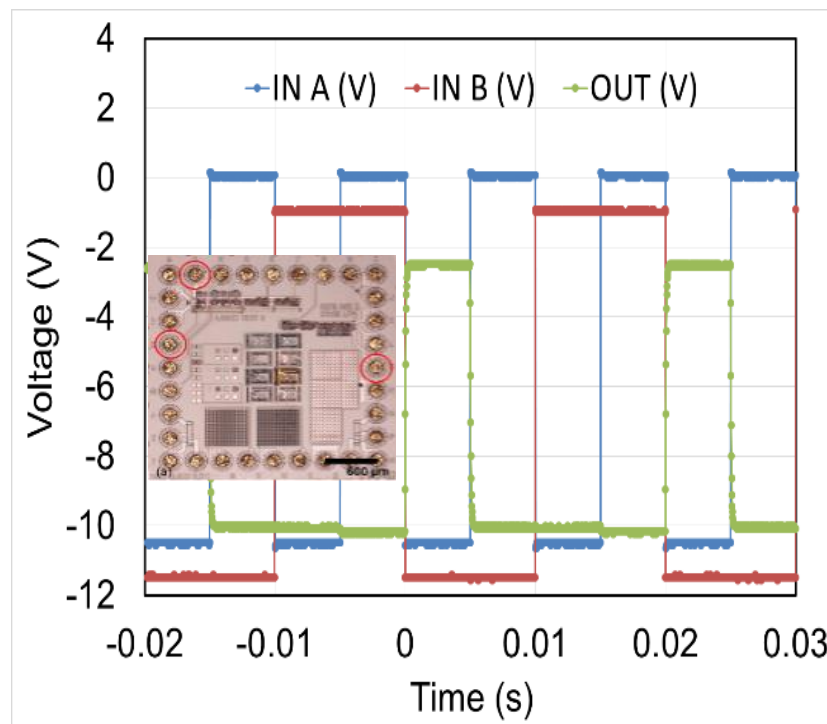


- Packaged SiC chip with Pt/HTCC alumina package and PCB
- PCB measures 2 inch x 2 inch, Pt traces co-fired with alumina
- 1 mil Au alloy wire thermo-sonically bonded

Test with SiC ICs at High Temperature



Input (dark) and output (blue) waveforms of OPAMP in closed loop with SiC epi-resistors of ratio of 8 to 1
 500 °C air ambient after 3736 hours



Input (red and blue) and output (green) waveforms of a NOR logic gate after 143.5 hours test in 700 °C air ambient

D. J. Spry, P. G. Neudeck, L.-Y. Chen, D. Lukco, C. W. Chang, G. M. Beheim, "Experimental Durability Testing of 4H SiC JFET Integrated Circuit Technology at 727 °C," in process.



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Summary

- A prototype 32-I/O high temperature co-fired Pt/92% alumina package was designed, fabricated, electrically characterized
- This package was tested with SiC integrated circuits at 500 °C, and 700°C for the first time
- DC and AC electrical parasitic parameters of neighboring I/Os of this package characterized between room temperature and 500 °C
 - At 500 °C the DC resistance between neighboring I/Os is above 1 GΩ
 - AC parasitic capacitance between neighboring I/Os at temperatures $T \leq 500$ °C in the frequency range from 120Hz and 1MHz is below 1.5pF, and parasitic AC resistance is over 20 MΩ
 - A co-fired Pt/92% alumina PCB demonstrated
 - Packaged SiC ICs successfully tested at 500 °C for over 3736 hours, and over 140 hours at 700°C
- Good wire-bonding yields achieved, Au wire-bonding reliability on package pads to be further improved by Au coating on Pt
- More long term and thermal cycling tests for future

Thank You Very Much for Your Attention!

Acknowledgements

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